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<p>(21) International Application Number: PCT/GB98/01145</p> <p>(22) International Filing Date: 20 April 1998 (20.04.98)</p> <p>(30) Priority Data: 9725205.0 29 November 1997 (29.11.97) GB</p> <p>(71) Applicant: BOOKHAM TECHNOLOGY LTD. [GB/GB]; 90 Milton Park, Abingdon, Oxon OX14 4RY (GB).</p> <p>(72) Inventors: DAY, Ian; 12a Saint Andrew Lane, Old Headington, Oxford OX3 9DP (GB). MCKENZIE, James, Stuart; Flat 6, 67-69 The Greenway, Uxbridge, Middlesex UB8 2PL (GB).</p> <p>(74) Agent: UNWIN, Stephen, Geoffrey; S.G. Unwin & Co., Brookfurlong Farmhouse, Islip, Oxford OX5 2TJ (GB).</p>		<p>(81) Designated States: AU, CA, CN, IL, JP, KR, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).</p> <p>Published <i>With international search report.</i> <i>With amended claims and statement.</i></p>
<p>(54) Title: METHOD OF AND INTEGRATED OPTICAL CIRCUIT FOR STRAY LIGHT ABSORPTION</p> <div data-bbox="454 1176 1169 1596"></div> <p>(57) Abstract</p> <p>An integrated optical circuit formed on an optically conductive substrate having light absorbing means comprising one or more doped areas (1) of the substrate where the doping concentration is greater than that of areas of the substrate forming the optical circuit (2) to absorb stray light in the substrate which is not guided by components of the optical circuit.</p>		

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METHOD OF AND INTEGRATED OPTICAL CIRCUIT FOR STRAY LIGHT ABSORPTION

TECHNICAL FIELD

This invention relates to a method of absorbing stray light in an integrated optical circuit and to an integrated optical circuit comprising light absorbing means for absorbing stray light.

BACKGROUND ART

In the design of integrated optical circuits there is often a need to deal with light which is not guided by the components forming the circuit. This stray light, which can arise from many sources, such as fibre or laser couplers, scattering from waveguide couplers and bends or from scattering beam dumps, can have a severe impact on the performance of devices which employ these components. The stray light in the optical chip can enter devices on the chip, and output fibres and may severely limit the performance of these devices.

Conventional methods of dealing with this problem include physically arranging devices on an integrated optical chip such that stray light cannot enter sensitive parts of the chip and the use of isolation trenches to keep stray light away from certain parts of the chip.

The limitation of these approaches is that they do not remove the stray light from the integrated optical chip, but instead attempt to minimise the problem of having stray light within the chip.

DISCLOSURE OF THE INVENTION

According to a first aspect of the invention, there is provided a method of absorbing stray light in an integrated optical circuit formed on an optically conductive substrate comprising the step of doping selected areas of the substrate so as to increase the absorption of light which is not guided by components of the optical circuit in those areas.

According to a second aspect of the invention, there is provided an integrated optical circuit formed on an optically conductive substrate comprising light absorbing means for absorbing stray light in the substrate, the light absorbing means comprising one or more doped areas of the substrate where the doping concentration is greater than that of areas of the substrate forming the optical circuit to absorb stray light in the substrate which is not guided by components of the optical circuit.

Other features of the invention will be apparent from the following description and from the subsidiary claims of the specification.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will now be further described, merely by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a schematic diagram illustrating the use of doped areas adjacent a Y-junction in a waveguide in accordance with the invention;

Figure 2 is a schematic diagram illustrating the use of doped areas adjacent a coupling between a laser diode and a waveguide in accordance with the invention;

Figure 3 is a schematic diagram illustrating the use of a doped area between a light source and a light detector in accordance with the invention.

Figure 4 is a graph showing the length of doped area against the absorption loss for two given wavelengths, for a particular concentration of n-type doping; and

Figure 5 is a graph showing the length of doped area against the absorption loss for two given wavelengths for a particular concentration of p-type doping.

BEST MODE OF CARRYING OUT THE INVENTION

It is known that free charge carriers arising from ionised impurity atoms (i.e. doping atoms) change the refractive index and increase the linear optical absorption coefficient of silicon at wavelengths commonly used in telecommunications, i.e. 1310nm and 1550nm. Detailed measurements have been published in the literature (see for example R.A.Soref and B.R.Bennett "Electro-optical Effects in Silicon". IEEE Journal of Quantum Electronics QE-23 (1) p.123 1987) for common impurity atoms such as Boron (a p-type dopant) and Phosphorous (an n-type dopant). This effect is used in integrated optical switches and transducers by arranging for free charge carriers to be injected into a waveguide upon the application of a voltage across the waveguide.

In the present invention this effect is used to provide light absorbing means in an optical chip to absorb stray light in the chip.

By doping selected areas of the chip, stray light in the chip can be removed by the process of free charge carrier absorption so dealing directly with the problem of stray light and the limitations this can cause on device performance.

The doped areas may be formed in a variety of locations such as adjacent a coupling between a light source or optical fibre and a waveguide, adjacent a bend in a waveguide, adjacent a junction in a waveguide or a coupling between waveguides, adjacent a beam dump and between a light source and a light sensor. In general, the doped regions are positioned so as to prevent light from any source of stray light reaching another component in the circuit which is susceptible to such light.

Figure 1 illustrates the use of doped regions 1 adjacent a Y-junction 2 in a waveguide. The doped regions 1 are preferably formed in areas where they will absorb a substantial amount of the stray light emanating from the junction,

e.g. adjacent the outer edges of the arms of the Y-junction and in the area between the arms of the Y-junction.

Figure 2 illustrates the use of doped regions 1 adjacent a coupling between a laser diode 3 and a waveguide 4. The laser diode 3 is aligned with the waveguide 4 so the majority of the light emitted by the diode is directed along the waveguide. Nevertheless, a certain amount of light diverging from the laser diode 3 does not enter the waveguide 3 and produces stray light in the optical chip. The doped regions 1 are formed on either side of the waveguide in positions where they will intercept and absorb a substantial proportion of this stray light. A similar arrangement may be used where the light source is an optical fibre instead of the laser diode 3.

The doped regions 1 shown in Figures 1 and 2 may typically be about 20 microns wide and about 100 microns long.

Figure 3 illustrates the use of a doped region 1 between a laser diode 5 and a photo diode 6, e.g. on a transceiver chip. The doped region 1 is positioned so as to intercept stray light which may find its way from the laser diode 5 to the photo diode 6. The doped region 1 is formed so as to encircle or surround the laser diode 5 and/or the photo diode 6, except in the region(s) where light from the diode(s) is directed into or received from a waveguide 7, so as to optically isolate the diode(s) apart from the designated light exit or entrance. By isolating the photo diode 6 from the light source 5 in this way, its sensitivity is increased. In an alternative arrangement (not shown) the doped region may simply comprise an elongate band between the laser diode 5 and the photo diode 6. The various sections of the doped region 1 in Figure 3 would also typically be about 20 microns wide and 100 microns long.

The doping concentration required and the size of the doped regions will depend on many factors such as the type of substrate used, the type of dopant used, and the performance requirements of the device.

Figure 4 shows a graph of the length of doped area through which the stray light passes and the absorption loss for the two wavelengths 1310nm and 1550nm for a p doping concentration of $1.6 \times 10^{20} \text{cm}^{-3}$ of phosphorous atoms in a silicon substrate. This graph has been calculated using data published in the literature referred to above. The graph shows that with a doping length of 7 microns (for the wavelength 1310nm) and 10 microns (by extrapolation, for the wavelength 1550nm) a significant level of absorption (in excess of 60dB) occurs.

The graph also shows that even a short length of dopant, e.g. about 1 micron, produces a useful degree of absorption (about 10dB).

Figure 5 shows a similar graph using a lower doping concentration of $1.6 \times 10^{19} \text{cm}^{-3}$ of boron atom. This example does not provide such an efficient absorber as that in Figure 4 (due to the lower concentration of the dopant and the lower absorption per unit volume of boron compared to phosphorous) but, nevertheless, shows that a useful level of absorption, e.g. 10dB or more, can be achieved using a doping region having a length of between 20 and 40 microns.

Other n and p-type dopants may be used in place of or in addition to phosphorous and boron.

The examples given above relate to a silicon substrate, e.g. a silicon-on-insulator (SOI) chip. Such chips are manufactured to given specifications for the purity of the silicon to enable efficient devices to be formed therefrom. The "background" impurity level of the silicon in such a device is typically in the

order of 10^{15}cm^{-3} . The doping concentration of the doped regions 1 should preferably be at least 10^{16}cm^{-3} and most preferably at least 10^{19} or 10^{20}cm^{-3} .

The doping level used should preferably be sufficient to enable absorption of at least 10dB, and preferably 50dB or more, to be achieved using doping regions less than 200 microns in length and preferably 40 microns or less and most preferably 20 microns or less.

With a silicon-on-insulator chip, the silicon layer typically has a thickness of 2 - 8 microns and rib waveguides typically having a width of about 4 microns, are formed by etching a recess in the silicon layer on each side of the rib. The doped regions 1 formed on either side of the rib, e.g. as shown in Figures 1 and 2, may then be formed by diffusing dopant into the recess on either side of the rib. In other cases, e.g. when the doped region is adjacent a photo diode, e.g. as shown in Figure 3, it is formed by diffusing into the silicon layer adjacent the diode without the prior formation of a recess.

The doped regions are typically formed by subjecting the relevant regions to an atmosphere containing the dopant atoms at an elevated temperature. Following this, the device is heated again in an oxygen atmosphere to diffuse the dopant further into the chip and form an oxide layer over the chip. It is obviously desirable for the dopant to extend through the entire depth of the optical layer, e.g. the silicon layer in an SOI substrate, to avoid the possibility of stray light escaping underneath the doped regions. The concentration of dopant will generally vary with depth in the optical layer, e.g. by a factor of 10 per micron of depth, and in the preferred arrangement the minimum level of doping (usually at the bottom of the layer 1) should be of a sufficient level to provide the required degree of absorption.

The doped regions may, in many cases, be formed close to the relevant source of stray light to maximise the amount of light absorbed. The regions may, for

instance, be formed less than 5 microns from the relevant source, e.g. a rib waveguide etc. as shown in Figures 1 and 2, but should not be formed so close as to interfere with the operation of the relevant component.

Such doped regions can conveniently be formed at the same time as other components of the circuit are fabricated, e.g. modulators, and their position can be accurately determined by standard photolithographic techniques.

In some applications it may be possible to form doped regions over the entire area of a chip occupied by the integrated optical circuit apart from the areas in which the components of the optical circuit themselves are formed in order to maximise the absorption of stray light. The doped regions will, however, increase the electrical conductivity of the chip so in cases where it is not desirable to create an electrical path between components of the optical circuit, isolated doping regions such as those described above should be used.

The doped regions preferably all comprise the same type of dopant, i.e. either n-type or p-type, so as to avoid forming unwanted diodes between n and p-type regions. For the same reason, the doped regions used for absorption should not be formed too close to the n and p-type doped regions provided for other purposes.

It will be appreciated that the use of doped regions as light absorbing means, as described above, enables the problems caused by stray light in the optical chip to be significantly reduced. This enables optical circuits to be designed independently of stray light considerations and enables the available space on a chip to be used much more efficiently and so enable more compact devices to be fabricated.

CLAIMS

1. A method of absorbing stray light in an integrated optical circuit formed on an optically conductive substrate comprising the step of doping selected areas of the substrate so as to increase the absorption of light which is not guided by components of the optical circuit in those areas.
2. A method as claimed in Claim 1 in which the substrate comprises silicon.
3. A method as claimed in Claim 1 in which the dopant is diffused or implanted into the silicon substrate so that the concentration of dopant exceeds 10^{16}cm^{-3} through the thickness of the substrate and preferably exceeds 10^{19}cm^{-3} through the substrate.
4. A method as claimed in Claim 1, 2 or 3 in which the selected areas comprise one or more of the following areas: adjacent a coupling between a light source or optical fibre and a waveguide, adjacent a bend in a waveguide, adjacent a junction in a waveguide or a coupling between waveguides, adjacent a beam dump, around a light source, between a light source and a light sensor.
5. An integrated optical circuit formed on an optically conductive substrate having light absorbing means comprising one or more doped areas of the substrate where the doping concentration is greater than that of areas of the substrate forming the optical circuit to absorb stray light in the substrate which is not guided by components of the optical circuit.
6. An integrated optical circuit as claimed in Claim 5 in which an n-type dopant is used, preferably phosphorous.

7. An integrated optical circuit as claimed in Claim 5 in which a p-type dopant is used, preferably boron.
8. An integrated optical circuit as claimed in Claim 5, 6 or 7 in which the doped areas are provided in one or more of the following locations: adjacent a coupling between a light source or optical fibre and a waveguide, adjacent a bend in a waveguide, adjacent a junction in a waveguide or a coupling between waveguides, adjacent a beam dump, around a light source, between a light source and a light sensor.
9. An integrated optical circuit as claimed in any of Claims 5 to 8 in which the doped region has a length of at least one micron and preferably at least 7 microns.
10. An integrated optical circuit as claimed in any of Claims 5 to 9 in which the doped region extends through the depth of the optically conductive substrate.
11. An integrated optical circuit as claimed in any of Claims 5 to 10 formed on a silicon-on-insulator chip.
12. An integrated optical circuit as claimed in Claim 11 in which the said one or more doped areas are formed using phosphorous as the dopant.
13. An integrated optical circuit as claimed in Claim 12 in which the dopant level is in excess of 10^{16}cm^{-3} and preferably at least 10^{20}cm^{-3} .
14. An integrated optical circuit as claimed in Claim 11 in which the said one or more doped areas are formed using boron as the dopant.

15. An integrated optical circuit as claimed in Claim 14 in which the dopant level is in excess of 10^{16}cm^{-3} and preferably at least 10^{19}cm^{-3} .

AMENDED CLAIMS

[received by the International Bureau on 24 March 1999 (24.03.99);
original claims 1 and 5 amended; remaining claims unchanged (3 pages)]

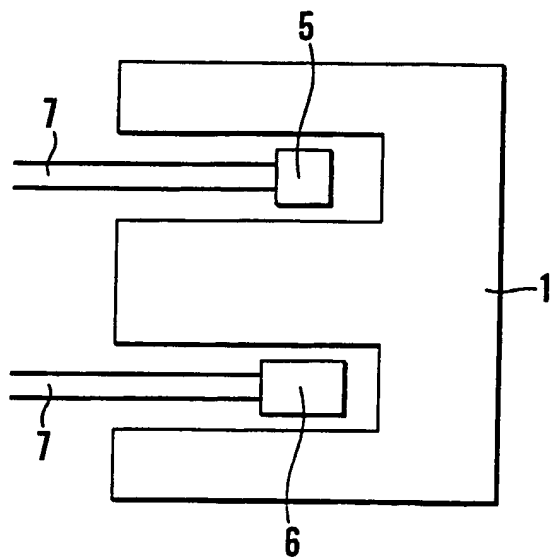
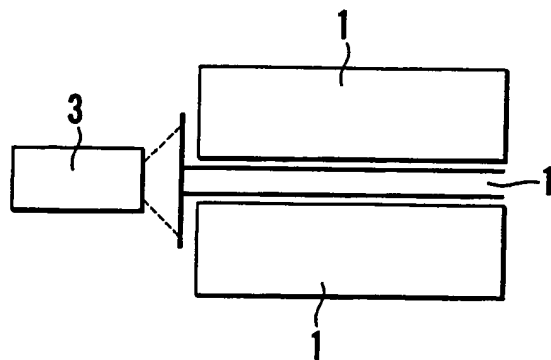
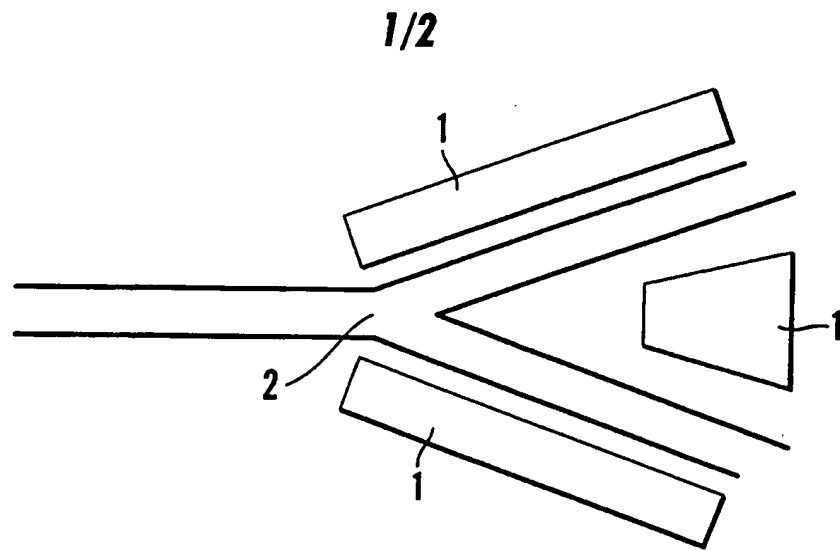
1. A method of absorbing stray light in an integrated optical circuit formed on an optically conductive substrate comprising the step of doping selected areas of the substrate so as to increase the absorption of stray light which is not guided by components of the optical circuit in those areas of the substrate, the doped areas being spaced from the said components so as not to interfere with their operation.
2. A method as claimed in Claim 1 in which the substrate comprises silicon.
3. A method as claimed in Claim 1 in which the dopant is diffused or implanted into the silicon substrate so that the concentration of dopant exceeds 10^{16}cm^{-3} through the thickness of the substrate and preferably exceeds 10^{19}cm^{-3} through the substrate.
4. A method as claimed in Claim 1, 2 or 3 in which the selected areas comprise one or more of the following areas: adjacent a coupling between a light source or optical fibre and a waveguide, adjacent a bend in a waveguide, adjacent a junction in a waveguide or a coupling between waveguides, adjacent a beam dump, around a light source, between a light source and a light sensor.
5. An integrated optical circuit formed on an optically conductive substrate having light absorbing means in selected areas of the substrate comprising one or more doped areas where the doping concentration is greater than that of areas of the substrate forming the optical circuit so as to absorb stray light in the substrate which is not guided by components of the optical circuit, the doped areas being spaced from the said components so as not to interfere with their operation.

6. An integrated optical circuit as claimed in Claim 5 in which an n-type dopant is used, preferably phosphorous.
7. An integrated optical circuit as claimed in Claim 5 in which a p-type dopant is used, preferably boron.
8. An integrated optical circuit as claimed in Claim 5, 6 or 7 in which the doped areas are provided in one or more of the following locations: adjacent a coupling between a light source or optical fibre and a waveguide, adjacent a bend in a waveguide, adjacent a junction in a waveguide or a coupling between waveguides, adjacent a beam dump, around a light source, between a light source and a light sensor.
9. An integrated optical circuit as claimed in any of Claims 5 to 8 in which the doped region has a length of at least one micron and preferably at least 7 microns.
10. An integrated optical circuit as claimed in any of Claims 5 to 9 in which the doped region extends through the depth of the optically conductive substrate.
11. An integrated optical circuit as claimed in any of Claims 5 to 10 formed on a silicon-on-insulator chip.
12. An integrated optical circuit as claimed in Claim 11 in which the said one or more doped areas are formed using phosphorous as the dopant.
13. An integrated optical circuit as claimed in Claim 12 in which the dopant level is in excess of 10^{16}cm^{-3} and preferably at least 10^{20}cm^{-3} .
14. An integrated optical circuit as claimed in Claim 11 in which the said one or more doped areas are formed using boron as the dopant.

15. An integrated optical circuit as claimed in Claim 14 in which the dopant level is in excess of 10^{16}cm^{-3} and preferably at least 10^{19}cm^{-3} .

STATEMENT UNDER ART. 19(1)

This invention relates to the formation of light absorbing areas by doping selected areas of the substrate. The position and location of these areas can thus be controlled and they can be accurately formed using well-known processing techniques. The invention is also applicable to optical circuits in which the components of the circuit, e.g. waveguides, and the substrate are formed of the same material, e.g. silicon. The prior art does not provide these advantages. The doped areas are formed so they are spaced a sufficient distance from the optical components so as not to interfere with their operation, e.g. so as not to attenuate an optical signal transmitted along a waveguide (as a proportion of the signal is carried in areas of the substrate adjacent the component structure, such as the waveguide ridge or core, used to guide the wave). This overcomes a significant disadvantage of the prior art.



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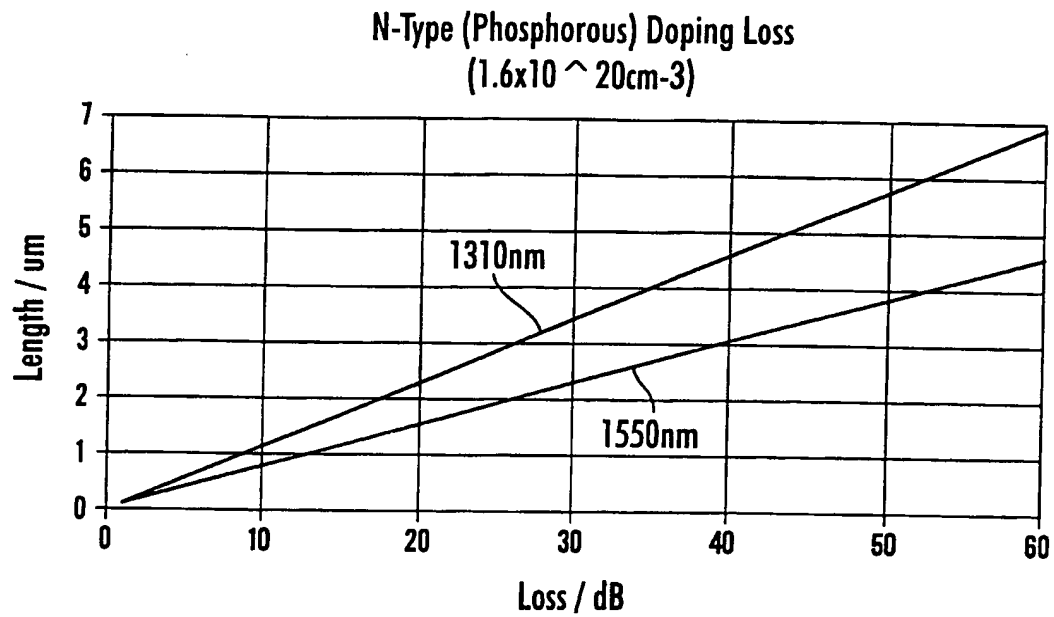


Fig.4

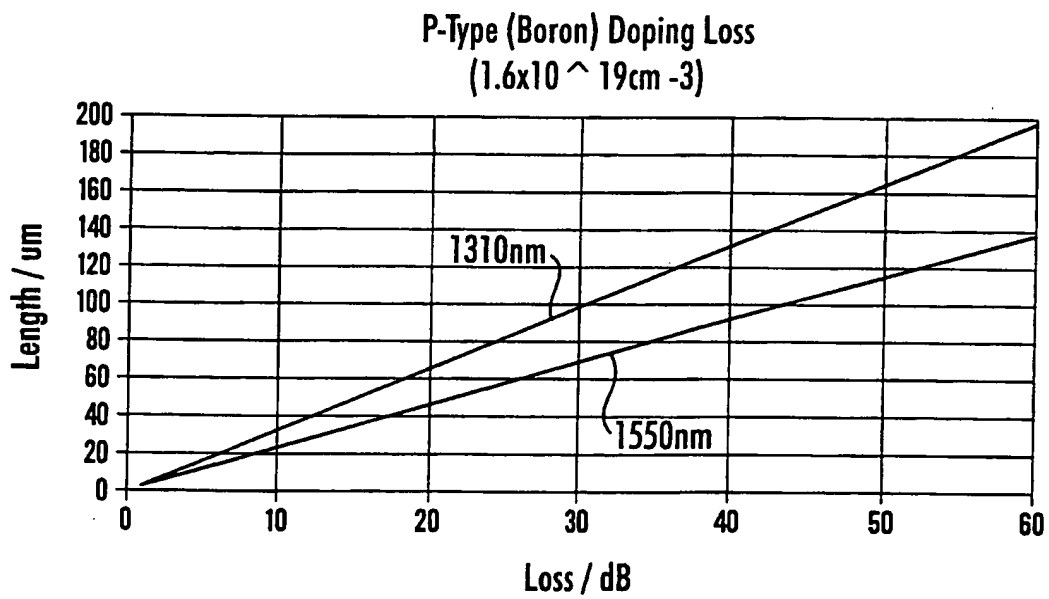


Fig.5

INTERNATIONAL SEARCH REPORT

International Application No

PCT/GB 98/01145

A. CLASSIFICATION OF SUBJECT MATTER

IPC 6 G02B6/12

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 G02B

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Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	PATENT ABSTRACTS OF JAPAN vol. 016, no. 266 (P-1371), 16 June 1992 & JP 04 067103 A (BROTHER IND LTD), 3 March 1992, see abstract	1,5,9,10
A	R.A. SOREF ET AL.: "Electrooptical Effects in Silicon" IEEE J. QUANTUM ELECTRON., vol. QE-23, no. 1, 1 January 1987, USA, pages 123-129, XP002072376 cited in the application see paragraph IV; figures 5,7,12-14	3,6,7, 12-15
A	EP 0 397 337 A (PLESSEY OVERSEAS) 14 November 1990 see claims 1-5; figure 2	1,5
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☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the international search

23 July 1998

Date of mailing of the international search report

20/08/1998

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 617 301 A (NIPPON ELECTRIC CO) 28 September 1994 see column 3 - column 4; figures 2,3 ---	6,7,12, 14
A	EP 0 080 945 A (FUJITSU LTD) 8 June 1983 see page 5 - page 17; figures 5-8 ---	4,8
A	US 5 093 884 A (GIDON PIERRE ET AL) 3 March 1992 see column 4, line 47 - line 66 see column 7, line 10 - column 11, line 35; figures 1,2 -----	5,6,12, 14

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/GB 98/01145

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0397337 A	14-11-1990	GB 2231683 A JP 3004205 A	21-11-1990 10-01-1991
EP 0617301 A	28-09-1994	JP 2637891 B JP 6281828 A US 5408569 A	06-08-1997 07-10-1994 18-04-1995
EP 0080945 A	08-06-1983	JP 58170057 A JP 1039231 B JP 1556196 C JP 58093390 A US 4607368 A	06-10-1983 18-08-1989 23-04-1990 03-06-1983 19-08-1986
US 5093884 A	03-03-1992	FR 2663435 A CA 2044414 A DE 69123176 D DE 69123176 T EP 0461991 A JP 5072432 A	20-12-1991 14-12-1991 02-01-1997 15-05-1997 18-12-1991 26-03-1993